L Number	Hits	Search Text	DB	Time stamp
1	677	configurat$4 same bitstream	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:03
2	248	(configurat$4 same bitstream) and code and instruct$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:33
3	142	((configurat$4 same bitstream) and code and instruct$4) and transform$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:06
5	17	(((configurat$4 same bitstream) and code and instruct$4) and pld) and segment	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:07
4	67	((configurat$4 same bitstream) and code and instruct$4) and pld	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:14
6	27	(((configurat$4 same bitstream) and code and instruct$4) and pld) and arrange$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:32
7	29474	code same segment	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:33
8	76	(configurat$4 same bitstream) and (code same segment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:35
10	60	((configurat$4 same bitstream) and (code same segment)) and instruct$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:34
11	2	(configurat$4 same bitstream) same (code same segment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:40
12	9	"6023755"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/15 19:41

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1	US 20040174187 A1	20040909	13	FPGA architecture with mixed interconnect resources optimized for fast and low-power routing and methods of utilizing the same	326/41
2	US 20040060032 A1	20040325	26	Automated system for designing and developing field programmable gate arrays	716/16
3	US 20040030975 A1	20040212	9	Methods of resource optimization in programmable logic devices to reduce test time	714/725
4	US 20030229877 A1	20031211	34	System and method for configuring analog elements in a configurable hardware device	716/16
5	US 20030144828 A1	20030731	237	Hub array system and method	703/21
6	US 20030078752 A1	20030424	14	SYSTEM AND METHOD FOR TESTING A CIRCUIT IMPLEMENTED ON A PROGRAMMABLE LOGIC DEVICE	702/120
7	US 20030074489 A1	20030417	92	Measurement system with modular measurement modules that convey interface information	710/1
8	US 20030046380 A1	20030306	90	Measurement module interface protocol database and registration system	709/223
9	US 20030040881 A1	20030227	91	Measurement system including a programmable hardware element and measurement modules that convey interface information	702/123
10	US 20020152060 A1	20021017	207	Inter-chip communication system	703/17
11	US 20020085021 A1	20020704	28	Dynamically adaptive multimedia application program interface and related methods	345/716
12	US 20020083331 A1	20020627	50	Methods and systems using PLD-based network communication protocols	713/200

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13	US 20020080784 A1	20020627	50	Methods and systems using PLD-based network communication protocols	370/389
14	US 20020080771 A1	20020627	50	Methods and systems using PLD-based network communication protocols	370/352
15	US 20020067369 A1	20020606	28	Application program interface (API) facilitating decoder control of accelerator resources	345/716
16	US 20020065952 A1	20020530	29	Extensible multimedia application program interface and related methods	719/328
17	US 20020063792 A1	20020530	28	Interface and related methods facilitating motion compensation in media processing	348/416.1
18	US 20010047509 A1	20011129	28	Modular design method and system for programmable logic devices	716/18
19	US 6785873 B1	20040831	191	Emulation system with multiple asynchronous clocks	716/4
20	US 6760899 B1	20040706	11	Dedicated resource placement enhancement	716/16
21	US 6754763 B2	20040622	225	Multi-board connection system for use in electronic design automation	710/317
22	US 6748368 B1	20040608	9	Proprietary core permission structure and method	705/500
23	US 6725441 B1	20040420	14	Method and apparatus for defining and modifying connections between logic cores implemented on programmable logic devices	716/16
24	US 6665766 B1	20031216	11	Adaptable configuration interface for a programmable logic device	710/305
25	US 6651225 B1	20031118	179	Dynamic evaluation logic system and method	716/4

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27	US 6618686 B2	20030909	14	System and method for testing a circuit implemented on a programmable logic device	702/120
28	US 6617876 B1	20030909	11	Structures and methods for distributing high-fanout signals in FPGAs using carry multiplexers	326/41
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33	US 6510546 B1	20030121	15	Method and apparatus for pre-routing dynamic run-time reconfigurable logic cores	716/16
34	US 6496971 B1	20021217	14	Supporting multiple FPGA configuration modes using dedicated on-chip processor	716/16
35	US 6490712 B1	20021203	25	Method and system for identifying configuration circuit addresses in a schematic hierarchy	716/12

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53	US 6324676 B1	20011127	14	FPGA customizable to accept selected macros	716/16
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55	US 6308311 B1	20011023	19	Method for reconfiguring a field programmable gate array from a host	716/16
56	US 6305005 B1	20011016	10	Methods to securely configure an FPGA using encrypted macros	716/16
57	US 6297667 B1	20011002	57	Circuits and sequences for enabling remote access to and control of non-adjacent cells in a locally self-reconfigurable processing system composed of self-dual processing cells	326/41

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58	US 6278289 B1	20010821	14	Content-addressable memory implemented using programmable logic	326/40
59	US 6175530 B1	20010116	20	Method for detecting low power on an FPGA interface device	365/201
60	US 6134516 A	20001017	132	Simulation server system and method	703/27
61	US 6094063 A	20000725	20	Method for level shifting logic signal voltage levels	326/37
62	US 6047115 A	20000404	13	Method for configuring FPGA memory planes for virtual hardware computation	716/16
63	US 6026230 A	20000215	131	Memory simulation system and method	703/13
64	US 5892961 A	19990406	15	Field programmable gate array having programming instructions in the configuration bitstream	712/10
65	US 5872529 A	19990216	11	Dynamic datastream compression/decompression	341/59
66	US 5773993 A	19980630	15	Configurable electronic device which is compatible with a configuration bitstream of a prior generation configurable electronic device	326/38
67	US 5068603 A	19911126	68	Structure and method for producing mask-programmed integrated circuits which are pin compatible substitutes for memory-configured logic arrays	714/726